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ARTICLE

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Due to the intriguing optical and electronic properties, 2D materials are promising for next generation optoelectrinc and electric device applications. Discovering new 2D materials with novel physical properties are rewarding for this area. In this work, we systematically investigated the optoelectronic properties of 2D metal thiophosphate SnP_2S_6 with unique nanoporous structure. The intermediate bandgap makes SnP_2S_6 a good candidate as bothe the channel and gate dielectric materials in the transistor device. SnP_2S_6 showed good photoresponse properties. In addition, the MoS_2 transistor with SnP_2S_6 as dielectric layer shows a high dielectric constant($\approx$23), low subthreshold slope down to 69.4 mV/dec, and it presented a 0.1 pA scale leakage current, a threshold voltage as low as 1.1 V, a ON/OFF ratio reaching 10^7 and negligible hysteresis with high stability and reproducibility. This work would open up new avenues for the discovery of new metal thiophosphate systems for future device applications.

INTRODUCTION

The emergence of two-dimensional materials has brought new opportunities to the scientific and industrial fields. Due to the atomic ultrathin thickness, the quantum confinement effect in the thickness direction of two-dimensional materials is prominent, which demonstrated advantages of high carrier mobility, channel regulation capability and rich properties in force, heat, sound, light, electricity and magnetism[1-4]. As a result, novel electronic and optoelectronic devices based on 2D materials are developed and studied, and this is an active research field still today[5-7]. The rapid development of 2D materials is beneficial from the discovery of novel new 2D materials with intriguing physical properties. For example, the discovery of 2D $CuInP_2S_6$ brings the 2D ferroelectricity and related device application into the center of ferroelectric transistor and memory device field. The isolation of layered CrI_3 enables truly 2D ferromagnetic properties, attracting a lot of attention in the study of 2D magnetism. Layered ternary compounds such as Ta_2PdS_6[8], $In_2P_3S_9$[9], Bi_2O_2Se[10, 11], also provide new opportunities for the electronic and optoelectronic performance improvement for 2D material applications. There exists huge potential, opportunities as well as challenges for exploring new 2D material systems for the applications in future nanoelectronics and optoelectronics[12, 13].

For dielectric application, SiO_2 is used as dielectric layer typically, but traditional silicon-based field effect transistors (FETs) face various challenges when the device reduce to nanometer scale, the most prominent of which are reduced mobility and increased short-channel effects[14]. In order to mitigate these problems, novel dielectrics with remarkable properties begin to grow up. Advanced functional materials based on eco-friendly cellulose and sputtered multicomponent dielectrics can be processed under low temperature, and were reported to be implemented as high-capacitance gate dielectrics, which brings new insights into flexible and low-cost transistors and the need to meet the constraints for better band-offset matching[15, 16]. Moreover, 2D insulators are regarded as the ultimate solution for dielectric miniaturization[17]. Hexagonal boron nitride (h-BN) has been explored as the most promising 2D vdW dielectric layer, while novel 2D materials suitable for dielectric layer are rarely reported. However, the low dielectric constant ($\approx$ 5.0) and excessive leakage current make h-BN unsuitable for ultrascaled FETs with low power consumption[18, 19]. Therefore, it's important to find new materials to serve as reliable gate dielectric in FETs.

Among the various 2D material systems, the novel 2D metal thiophosphate MP_2X_6 (M = metal, X = S or Se)[20] has received much attention due to their intriguing physical properties, including magnetic, electronic, ferroelectric, and optical characteristics[21-23]. Among the most extensively studied systems contain the $Sn_2P_2S_6$ crystal with considerable piezo effect, proper ferroelectric and nonlinear optic properties [24, 25], MPS_3 as UV photodetector[26] which possess magnetic order[27], and $CuInP_2S_6$ heterostructure for non-

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volatile ferroelectric switches, memory devices and field-effect transistors[28, 29]. SnP_2S_6, a stable semiconductor material with a sizable indirect band gap of 2.23eV[30], is also of importance to be investigated as a member of this family. SnP_2S_6 exhibits a unique nonporous structure as it lacks half of the metal ions in the crystal structure of SnP_2S_6 compared to the parent $Sn_2P_2S_6$ structure. Due to the intrinsic 2D nanoporous structure, these days has witnessed more theoretical researches in SnP_2S_6[24, 30-32], despite the recent experimental study of strong nonlinear optical response related with its inversion symmetry broken structure[33, 34]. Recent theoretical study has predicted that SnP_2S_6 could have high carrier mobility[20], good switching stability, excellent insulation performance and gate-control ability. The measured dielectric constant is higher than the extensively used h-BN substrate[35]. Thus, it demonstrates great potential to be used as a channel or dielectric layer material in field effect transistors.

In this work, SnP_2S_6 is firstly proposed as dielectric layer, the electronic and optoelectronic characteristics of which have been systematically investigated. Field effect transistors with excellent performance are successfully constructed, which verifies the feasibility of SnP_2S_6 as dielectric layer material and provides new reliable building blocks for electronic devices based on 2D materials.

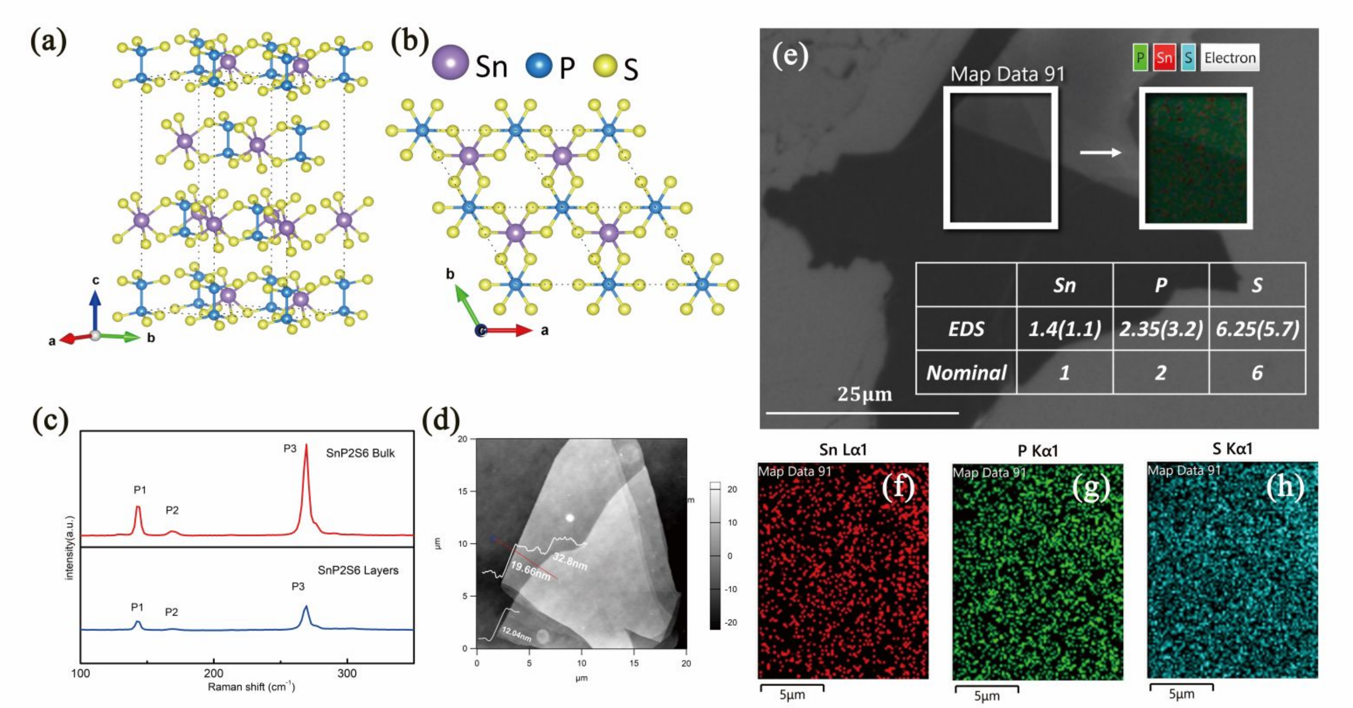

Fig 1 | **Characterization of 2D material SnP_2S_6.**
(a,b) Crystal structure of layered SnP_2S_6. **(a)** Side and **(b)** Top views. Purple, blue and yellow spheres represent Sn atoms, P atoms and S atoms, respectively. **(c)** Raman spectra of bulk and few-layer SnP_2S_6. **(d)** AFM topography of different-thickness SnP_2S_6. The thicknesses are around 12.04, 19.66 and 32.80 nm. **(e)** EDS results and elemental mappings of Sn **(f)**, P **(g)** and S **(h)** for typical SnP_2S_6 crystal, which shows homogenous distribution of the three elements.

Materials characterization

Layered SnP_2S_6 shows a rhombohedral layered structure (as shown in **Fig.1(a, b)**), which belongs to the R3 space group (No. 146) with rhombohedral symmetry[30, 36], and only contains one formula unit[20] of one metal cation Sn^{4+} and one anionic $[P_2S_6]^{4-}$. As depicted in **Fig.1(a), (b)**, the ternary SnP_2S_6 has a van der Waals layered structure and the interlayer spacing is about 0.65 nm, as reported in the literature[33]. Raman spectra were collected using a 532 nm laser in ambient conditions. As shown in **Fig.1(c)**, three distinct peaks P_1(≈142 cm^{-1}), P_2(≈168 cm^{-1}) and P_3(≈269 cm^{-1}) can be identified in both bulk and layered SnP_2S_6. Specifically, the three peaks are related to the internal stretching vibrations of S-P-S bonds[9], which are consistent with the previous report[33, 37]. As the thickness increases, the intensity alters while positions of all peaks hardly change, which might be due to the weak interlayer interaction. In addition, as shown in **Fig.1(e)**, it is noted that the atomic ratio of SnP_2S_6 sample is 14: 23.5: 62.5 and 11: 32: 57(totals 100), which is close to the stoichiometric ratio of 1:2:6 and the uniform distribution of elements Sn, P, and S are exhibited in **Fig.1(f)-(h)**, as confirmed by Energy Dispersive X-ray Spectroscopy characterization (details in **fig.S1**).

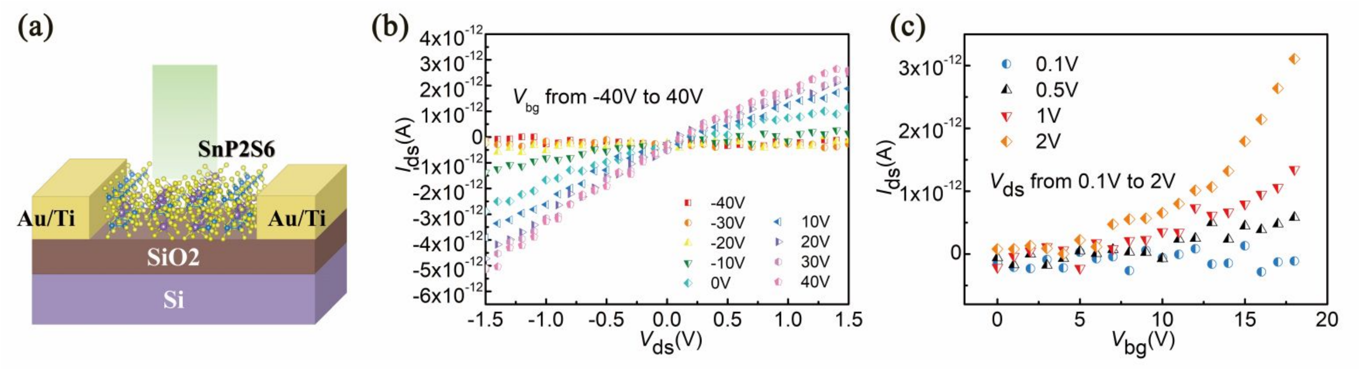

Fig 2 | **Electronic properties of back-gated FETs using SnP_2S_6 as the channel.**
(a) Schematic of the SnP_2S_6 photodetector on Si substrate, which provides the convenience of back gating. **(b)** Output curves (I_{ds}-V_{ds}) measured under V_{bg} from -40 V to 40 V. **(c)** I_{ds}-V_{bg} curves of SnP_2S_6 with different bias from 0.1 V to 2 V.

Optoelectronic properties of SnP_2S_6 thin flakes

SnP_2S_6 phototransistor is fabricated on the standard SiO_2/Si substrate (see methods part for details), and the schematic illustration of device is shown in **Fig.2(a)**. The transfer and output curve of the transistor based on SnP_2S_6 as the channel material are shown in **Fig.2(b), (c)**. A linear relationship between I_{ds} and V_{ds} was observed. However, the transistor shows a very low electron mobility, the mobility($\mu = Ld/W\varepsilon_0\varepsilon_r V_{ds} \times dI_{ds}/dV_{bg}$) under a drain bias of 2 V is calculated as $2.17 \times 10^{-5}\ \mathrm{cm^2V^{-1}s^{-1}}$. The electronic performance of the device with various thicknesses of SnP_2S_6 were also studied (detailed in **Supplementary fig.S2 and fig.S3**), demonstrating a similar insulating behaviour. The good insulating behaviour makes SnP_2S_6 suitable for a dielectric layer, as discussed in details in next section.

The I_{ds}-V_{ds} curves shown in **Fig.3(a)** are linear and symmetric for small bias voltages, indicating an ohmic like contact. The device shows an increase of drain current by several orders of magnitude as the device is illuminated. The typical optical image of the devices are shown in inset of **Fig.3(a)** and in **fig.S2**. Furthermore, the power dependence of the photocurrent is plotted with a log–log scale in **Fig.3(b)**. As the incident light power increases from 0.1 to 50 mW, the photocurrent I_{ph} increases monotonically from 8.3×10^{-12} to 1.2×10^{-10} A with a bias of 5 V, indicating that the photocurrent is linearly proportional to the incident light power following: $I_{ph} \sim P^{\beta}$. Moreover, as the gate voltage shifts from 0.1 to 5 V, the value of β increases from 0.23 to 0.44. The great loss of photocurrent represented by non-unity exponent relationship and low value of β suggest that the photocurrent is influenced by complex processes besides the absorption of photon, the generation of free carriers, recombination of the photogenerated free carriers, charge trapping by the defects and the charge impurities presented in SnP_2S_6 flake, scarcely lateral photoeffct[38] and the adsorbed molecules at SnP_2S_6/SiO_2 interface due to the large surface-to-volume ratio[39-41].

Meanwhile, the photoresponsivity R and photo-gain G at a drain voltage of V_{ds} = 5 V exhibit strong dependence on the illumination power, as shown in **Fig.3(c)**. The photoresponsivity R is one of the most important features for a photodetector[42]. $R = I_{ph}/PS$, where *P* is the incident light power density and *S* is the effective illuminated area. As shown in **Fig.3(c)**, the photoresponsivity increases with the decrease of light power, which is possibly attributed to the less frequent carrier recombination and longer carrier lifetime under weaker illumination. This is consistent with photoconductor-based photodetector previously reported[8, 43]. Photogain (G) is another parameter to evaluate the performance of a phototransistor, which can be calculated by the formula: $G = (I_{ph}/q)/(PS/h\nu) = h\nu R/q$,[44] where I_{ph} is the photocurrent, q is the electron charge, h is Planck's constant, ν is the light frequency, and R is responsivity. The value of *G* was stimated to reach up to 3.74 under the power of 0.1 mW.

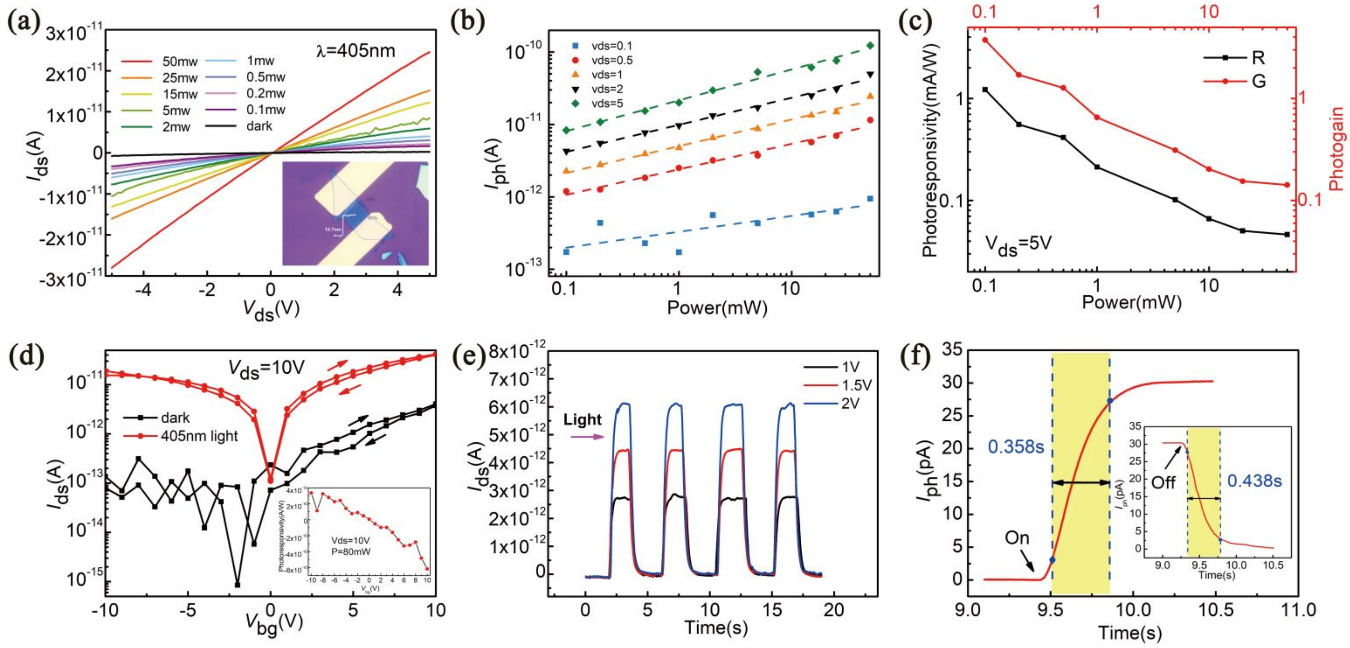

Fig 3 | **Optical properties of the SnP_2S_6 photodetector.**
(a) I_{ds}–V_{ds} curves of SnP_2S_6 under different light powers. Inset: The optical image of the device with thickness of 12.7 nm. **(b)** Photocurrent (I_{ph}) vary with light power and V_{ds}. **(c)** Photoresponsivity (R) and photogain (G) vary with light power. R_{max} = 1.22 mA/W, G_{max} = 3.74. **(d)** I_{ds}-V_{bg} curves at dark and under 405 nm light. The dark current could be reduced to pA. Under light condtions, current hysteresis box becomes little. Inset: Photoresponsivity vary with V_{bg}, under V_{ds}=10 V, P=80 mW. **(e)** The ON/OFF test of photocurrent under 532 nm light and the bias from 1 V to 2 V. The ON-OFF ratio >10^3. **(f)** The exponential fitting of the dynamic response of photocurrent for the rise and decay time. The deduced rise (τ_{rise}) and decay (τ_{decay}) time constants are about 0.358 s and 0.438 s.

The gate voltage dependence of the photoresponse of SnP_2S_6 is also investigated. The transfer curves under light on and off conditions are shown in **Fig.3(d)**, where an incident illumination power of 80 mW is applied. The curves show an increase of drain current by near two orders of magnitude once the device is illuminated, indicating that the photocurrent dominates in the entire operating range of the device. As can be seen from **Fig.3(d)**, the photocurrent shows an ambipolar behaviour with a large gate-tunability.

In order to study the stability and photoresponse speed of the SnP_2S_6 photodetector, the time-current curves with the 532 nm laser switching on and off was measured. For three different bias voltages (1V, 1.5V and 2V), as shown in **Fig.3(e)**, the time dependent photocurrent varies periodically with regular illumination, suggesting a stable and reversible photoresponse. The response speed is evaluated by a typical rise time/decay time, which is defined as the time over which the photocurrent increases from 10% to 90% (or decreases from 90 to 10% analogously) when the laser is switched on and off. **Fig.3(f)** shows the result of rise time and decay time of $\tau_{rise} = 0.358\ s$ and $\tau_{decay} = 0.438\ s$ for V_{ds} = 2 V, where the rising and falling parts of the curve can be fitted with an exponential function $I = I_0 + Ae^{t/\tau_{rise\ or\ decay}}$, where $\tau_{rise\ or\ decay}$ is rise or decay time constant.

Dielectric properties of SnP_2S_6 film

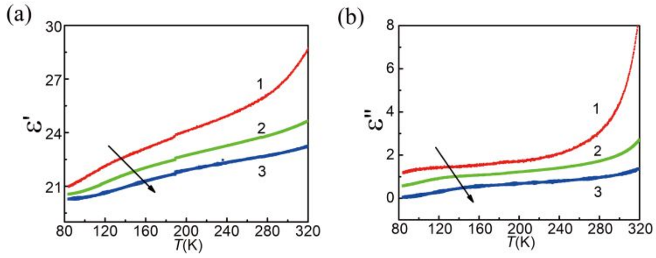

Fig. 4 | Temperature dependence of SnP_2S_6 crystal dielectric permittivity real **(a)** and imaginary **(b)** parts at frequencies 1(1 kHz), 2(10 kHz), 3(40 kHz).

We first studied the temperature dependence of the dielectric permittivity at different frequencies. For this, samples of SnP_2S_6 were used, obtained from the gas phase with a size of 5 x 5 x 0.05 mm^3. Silver paste deposited on opposite planes of the test sample was used as electrodes. The measurements were carried out in the frequency range 10 Hz to 50 kHz and in the temperature range 80 to 400 K. For research, we used a GW INSTEK LCR-819 meter and an immersed to liquid nitrogen cryostat with a temperature measurement accuracy of 0.001 K. The cooling rate was 0.1 K/min at a measuring field strength of 1 V/cm. As can be seen in **Fig.4(a), (b)**, when the SnP_2S_6 crystals are cooled, a monotonic decrease in the permittivity **(a)** and dielectric losses **(b)** are observed. At high temperatures, low frequency ε' and ε'' increase strongly, which is most likely due to an increase in the conductivity of the sample. The dielectric value of SnP_2S_6(≈23) is much higher than that of h-BN (≈ 5.0), which is comparable with or higher than those of traditional high-k oxide dielectrics such as Al_2O_3[45], HfO_2[46], ZrO_2[47].

Considering that SnP_2S_6 film has excellent insulating properties, good chemical stability and high dielectric constant, it shows great potential for integration into 2D FETs as a dielectric layer to modulate carrier density in a semiconducting channel. To demonstrate its advantages in this regard, we fabricate 2D FETs and evaluate the gating effect of SnP_2S_6 as top-gate dielectrics.

The well-studied 2D semiconductor MoS_2 was chosen as a representative channel material. Initially, we build MoS_2/SnP_2S_6 FETs on Si/SiO_2 (corresponding schematic is provided in **Supplementary fig.S5A)**, but the result shows that the hysteresis gap of the devices is too big (Supplementary **fig.S5C**). Here, in order to reduce the hysteresis gap, we use h-BN as the substrate, which can be prepared with a very uniform thickness and an atomically flat surface[48], and this method is proved to improve the performance of MoS_2 FETs as device substrate[49, 50]. The schematic illustration of our device is shown in **Fig.5(a) (**Optical image in **Supplementary fig.S6 and fig.S7D)**.

The thin-film 2D materials are obtained through a mechanical exfoliation process (see **Supplementary fig.S7A, B, C**). Through the process described in the methods, 7 devices based on SnP_2S_6/MoS_2 flakes of various thicknesses were fabricated. The optimal electric performance was observed in the devices with SnP_2S_6 of about 49.7 nm thickness (details **in Supplementary fig.S6 and fig.S8**). Meanwhile, a top-gate h-BN/MoS_2 FET was also fabricated for comparison according to the schematic in **Supplementary fig.S9C,** in which h-BN (with thickness of about 23.44 nm) is thinner than SnP_2S_6 (Optical and AFM image in **Supplementary fig.S6**). **Fig.5(b)** shows the top-gate transfer (I_{ds}-V_{tg}) characteristics measured for h-BN/ MoS_2 FET (the orange points) and four SnP_2S_6/ MoS_2 FETs on insulated h-BN substrate (see **Supplementary fig.S7D**). For the former one, a subthreshold slope (SS) value of 167.5 mV dec^{-1} and ON/OFF ratio of 10^5 was obtained. While for the latter, SnP_2S_6/ MoS_2 FETs, a small subthreshold slope (SS) value as low as 69.4 mV dec^{-1} for device 6 (Blue points) is achieved under a drain bias of 0.1 V, which is close to the limit value[51] of 60 mV dec^{-1}. The device could even reach high ON/OFF ratio of 10^7 and high carrier mobility of 28.498 $cm^2V^{-1}s^{-1}$ at higher drain bias (**Supplementary fig.S10 (A)**). The threshold voltage (V_t) is a parameter used to describe how much voltage is needed to initiate the channel conduction, which of the fabricated device is as low as -1.1 V (**Supplementary fig.S10 (B)**). The FETs with smaller SS value, low on voltage and low threshold voltage can achieve effective switching at a low V_{ds}, thereby reducing the leakage and power consumption of FETs devices. It's remarkable for our SnP_2S_6 to have such an excellent SS. In order to investigate the reason, we have carried out the following discussions. Through the contrast above, it is mostly possible that thicker SnP_2S_6 films of about 47.7 nm to 49.7 nm show best performance with greater possibility of applications. What's more, they have stronger gate control capability and low leakage current than those of 23.44 nm-thick h-BN.

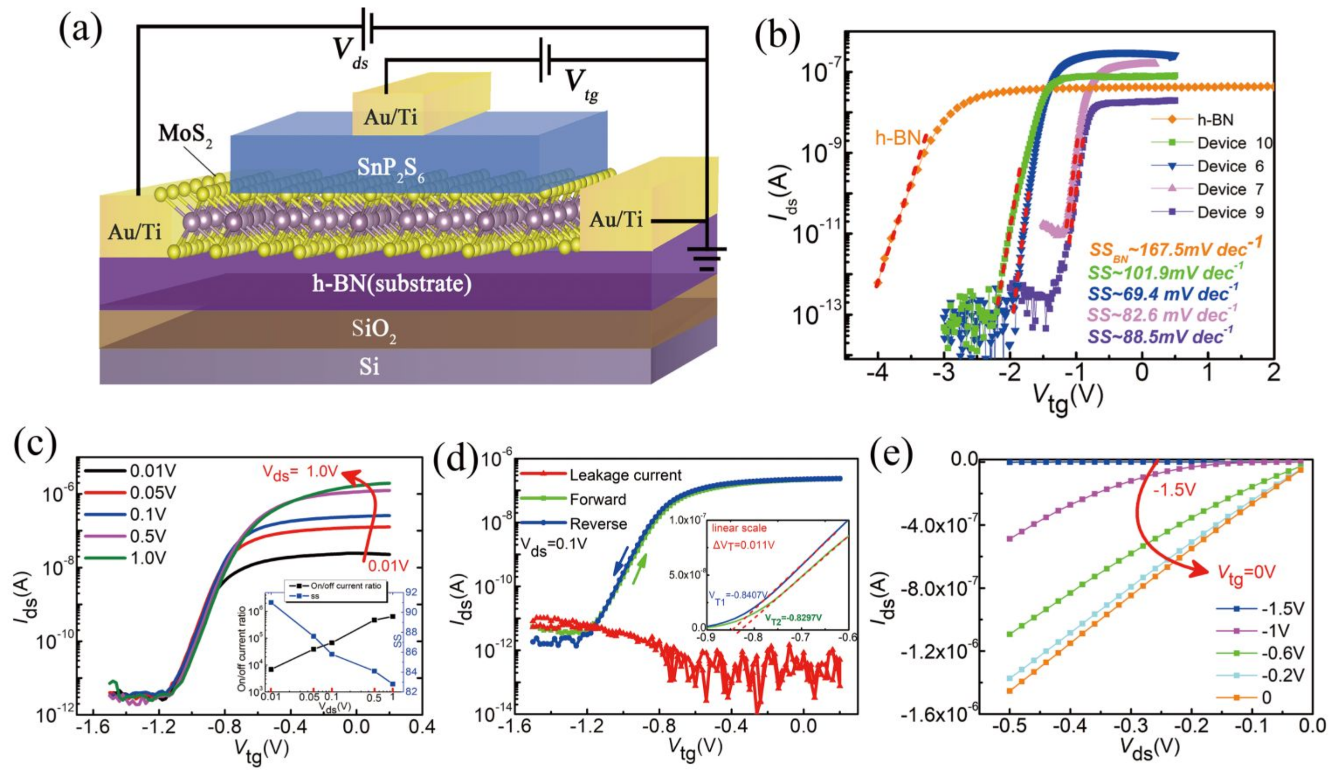

Fig. 5 | **Electronic properties of top-gated MoS_2 FETs using SnP_2S_6 as the gate dielectric. (a)** Schematic of SnP_2S_6/MoS_2 FETs using h-BN as substrate. **(b)** I_{ds}-V_{tg} curves of MoS_2 FETs at 300 K. The orange points represent h-BN/MoS_2 FET as contrasting device, in which h-BN is thinner than SnP_2S_6. Others are SnP_2S_6/MoS_2 FETs which exhibit subthreshold slope (SS) down to **69.4 mV/dec**. **(c-e)** show the best performance of

SnP_2S_6/MoS_2 FET (Device 7). **(c)** I_{ds}-V_{tg} characteristics measured at drain bias from 0.01 V to 1 V, the inset shows ON/OFF current ratio and SS extracted at different V_{ds}. **(d)** Double-sweep I_{ds}-V_{tg} curves show small hysteresis and leakage current, the inset is the current in linear scale (hysteresis gap $\Delta V_T \approx 0.011\ V$). **(e)** I_{ds}-V_{ds} characteristics measured at different V_{tg}.

which means larger capacitance value than h-BN in MoS_2 FETs ($C_{SnP_2S_6} > C_{h-BN}$). And since SnP_2S_6 is thicker than h-BN ($d_{SnP_2S_6} > d_{h-BN}$), according to the equation

$$C = \varepsilon_0 \varepsilon_r / d,$$

where C is capacitance value per unit area of the gate dielectric, ε_0 is permittivity of vacuum and ε_r is the relative dielectric constant. This confirms the high dielectric constant of SnP_2S_6 and advantages of integrating SnP_2S_6 nanosheet with semiconductor crystals to design FETs compared with h-BN, demonstrating the potential of 2D SnP_2S_6 as high-k dielectric for low power and miniaturized electronics.

As shown in **Fig.5(c,d)**, the typical SnP_2S_6/MoS_2 device exhibits high ON/OFF ration and steep SS simultaneously. The effect of the increasing drain bias, resulting in augmented drive current and steeper SS value, are displayed in (**Fig.5(c)**). It can be seen that the best transistor performance is achieved at V_{ds} = 1 V, with a maximum measured on-state current of $\sim 1\ \mu A$, ON/OFF current ratio close to 10^6, SS value as small as 82.6 mV dec^{-1} (inset of **Fig.5(c)**) and the leakage current as low as $\sim 10^{-11}\ A$ (**Fig.5(d)**), respectively. The corresponding hysteresis stability of the device was demonstrated in **Fig.5(d)**. To describe the hysteresis stability, we introduce the hysteresis gap (ΔV_T) , which is defined as the difference between the forward and reverse sweep threshold voltage[52]. As obtained in the linear scale in the inset of **Fig.5(d)**, $\Delta V_T = |V_{T1} - V_{T2}| \approx 0.011\ V$, was determined as low as 0.011 V , which is a fairy small value in FETs. However, the hysteresis gap is larger after two days in the glove box (Supplementary **fig. S11D, E, F**) and different hysteresis behaviours were observed in some of our devices (Supplementary **fig. S11A, B, C**). The hysteresis variation may be caused by flake quality or fabrication process in laboratory environment, which leads to charge trapping at the interface, adsorption/desorption of ambient molecules or atmospheric moisture in the exposed active layers[50, 53]. The small hysteresis could be indicated that the fabricated SnP_2S_6/MoS_2 device shows atomic flat and sharp interface. The corresponding output (I_{ds}-V_{ds}) characteristics measured for different V_{tg} (**Fig.5(e)**) show a linear I_{ds}-V_{ds} characteristics at low drain bias and saturated current at high drain bias.

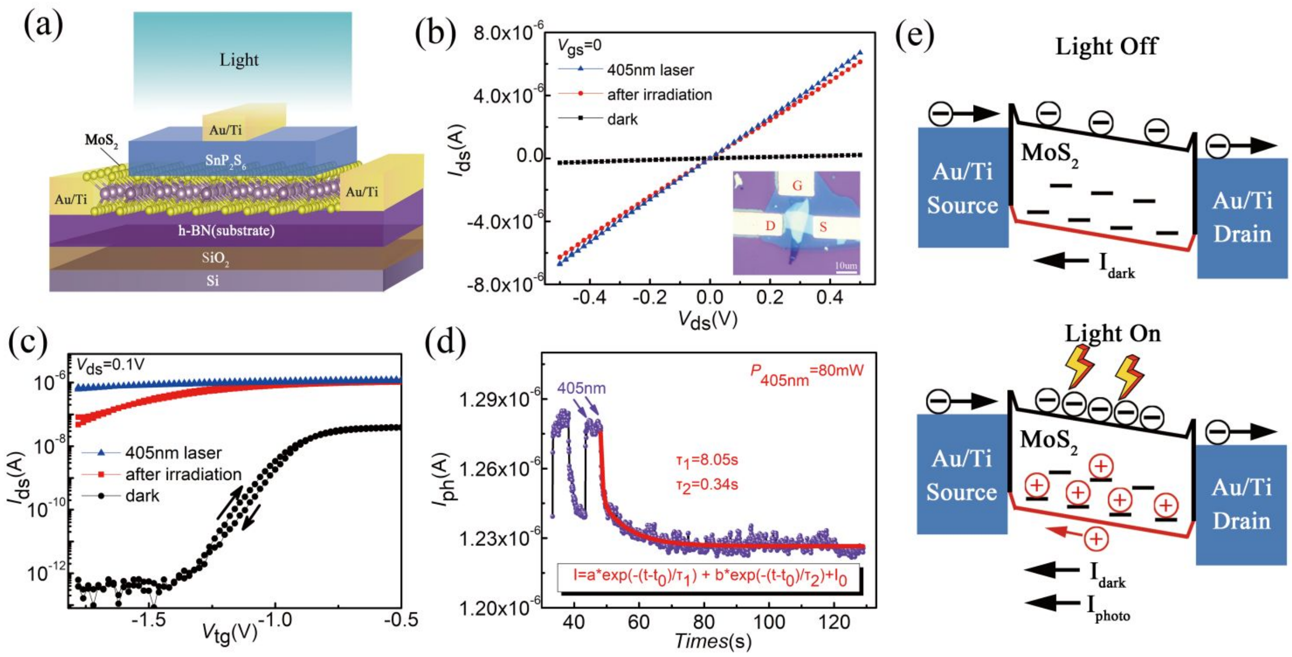

Fig. 6 | **Optical properties of top-gated SnP_2S_6/MoS_2 FETs. (a)** Schematic diagram of photogating dominated SnP_2S_6/MoS_2 FETs (**Device 9**). **(b)** Typical I_{ds}-V_{ds} characteristics of **Device 9** at dark (Black), under illumination (Blue) and after irradiation (Red), the inset is optical image of the FET. **(c)** I_{ds}-V_{tg} characteristics shows transfer curve shifts in negative V_{tg} direction under and after irradiation. **(d)** Photocurrent decay after a longer light pulse with longer ($\tau_1 \sim 8.05\ s$) and shorter ($\tau_2 \sim 0.34\ s$) time constants, which corresponds to **(b)** and **(c)**. **(e)** Band diagram of the device without (top panel) and with light (bottom panel), showing hole trapping in shallower and deeper trap states close to the valence band.

Breakdown electric field (V_{bd}) is another important parameter to evaluate the strength of insulating layer. To test the current leakage and breakdown threshold, SnP_2S_6 is sandwiched between two electrodes to perform a vertical device as shown in the inset of **fig.S12**. At room temperature, V_{bg} are fixed at 0 V, and V_{ds} is swept[54]. The I_{ds}-V_{ds} curve is plotted in **fig.S12**, where the initially low current increases slowly as the V_{ds} increase. The current increases dramatically as V_{ds} approaches V_{bd}. After breakdown, the device is permanently destroyed as a large current flows across SnP_2S_6. V_{bd} is estimated to be about 5 V (with thickness of 26.5 nm), and the corresponding breakdown electric field F_{bd} could be reach as high as 1.9 MV cm^{-1}.

Furthermore, to investigate the optoelectronic properties of our FETs, we put one of our SnP_2S_6/MoS_2 FETs on h-BN substrate (**Device 9**, its optical image in the inset of **Fig.6(b)**) under 405 nm laser irradiation of 80 mW. The output and transfer characteristics at dark (Black), under 405 nm irradiation (Blue) and after irradiation (Red) are separately depicted in. **Fig.6(b)** and **Fig.6(c)** separately. Under illumination, the output characteristic of the device remains linear while reducing the electrical resistance of the semiconductor caused by the photoconductive effect (PC effect), which is originated from the extra free carriers generated by the photon absorption (**Fig.6(b)**). Meanwhile, as shown in **Fig.6(c),** significant change in threshold voltage was observed when luminated by 405 nm light. The shifting of threshold voltage to the negative V_{tg} side is known as photogating effect (PG effect). PG effect is a phenomenon that photogenerated holes get trapped and then attract more electrons, thus gradually increasing the channel conductivity[55, 56].

In **Fig.6(c)**, compared with the initial device in dark condition, the Off-state current after irradiation is dramatically increased by more than five-orders of magnitude at the same V_{tg}, implying a long-time decay of photoconductive state. As shown in **fig.S13**, SnP_2S_6 has little effect on the optical response and persistent photocurrent of the device. Therefore, to explore the photocurrent decay of the device, we then check the transient characteristics by measuring the source-drain current at fixed V_{tg} = 0 V in **Fig.6(d)**. An abrupt increase in I_{ds} is observed as soon as illuminated under 405 nm laser, as a result of the photoexcitation, followed by a much slower current increase, namely the PG effect. A very slow decay of the current can be observed when the light was switched off. This is because the trapped charges in PG effect cause long sustained conductivity[56]. In order to quantify the trapping time constant, transient data was fitted with a biexponential equation of the type[57]

$$I = I_0 + Ae^{(t-t_0)/\tau_1} + Be^{(t-t_0)/\tau_2}$$

where τ_1 and τ_2 are two relaxation time constants, possibly corresponding to two different photoresponse mechanisms. The fast part is due to photoconductivity effect. The slow part could be regarded with the defect trapping or photogating effect. I_{ds} decays exponentially from $\sim 1.27\ \mu A$ in time and saturated after $35\ s$ with longer time constant $\tau_1 \sim 8.05\ s$ and shorter time constant $\tau_2 \sim 0.34\ s$. (See the detailed parameter values in **Supplementary Table 2** and time constants for different wavelengths in **Supplementary fig.S14**). The shorter decay component could be attributed to PC effect and shallower traps, while the longer decay component might be due to PG effect caused by deeper (middle gap) traps in **Fig.6(e)**, as elucidated by Furchi et al[55]. Simultaneously, the longer time constants of the devices on Si/SiO_2 FETs are $\sim 6.814\ s$ and $\sim 13.39\ s$, which are closed to $8.05 s$ in the FETs on h-BN (See Details in Supplementary **fig.S15**). Consequently, we infer that the long persistent photocurrent measured in our devices is not likely due to the traps at the MoS_2/SiO_2 or MoS_2/h-BN interface since our SnP_2S_6/MoS_2 FETs fabricated on h-BN which have very less charge trapping[50]. So it is conjectured that the defect trapping might be mainly originated from photo charge trapping associated with MoS_2 defects and the MoS_2/SnP_2S_6 interface, which causes the PG effect. Therefore, improving the quality of MoS_2 and optimizing the MoS_2/SnP_2S_6 interface can be an approach to decrease this phenomenon.

Finally, the good stability, reliability and reproducibility of the devices have been summarized as shown in **fig.S16, 17,18, 19.**

To compare the performance of SnP_2S_6 dielectric, the main set of achievements of the present study, such as dielectric constant, SS value and ON/OFF ratio were collected in Table 1. Compared with other new 2D dielectric materials, SnP_2S_6's high performance is comparable to or even better than those of these materials.

Table 1. Comparison of performance based on SnP_2S_6 with other new 2D dielectrics.

Materials	Dielectric constant	SS value [mV/dec]	ON/OFF ratio	Reference
Ta_2O_5	15.5	61	10^6	[58]
Bi_2SeO_5	21	75	10^5	[59]
CaF_2	8.43	90	10^7	[53]
$In_2P_3S_9$	24	88	10^5	[9]
Sb_2O_3	11.5	64	10^8	[60]
SnP_2S_6	23	69.4	10^7	This work

Conclusion

In this paper, we have systematically investigated the photoelectric and electrical properties of the novel 2D SnP_2S_6 crystal. Moreover, it was integrated into MoS_2 FETs to serve as top gate dielectric. The results demonstrate its excellent dielectric properties including large dielectric constant (≈23, compared with h-BN), a fairly small SS value (as low as 69.4 mV dec^{-1}), high ON/OFF ratio (reaching 10^7), negligible hysteresis, relatively high breakdown voltage (≈1.9 MV cm^{-1}). Due to its semiconductor nature, good photoelectric properties and good reliability and reproducibility (0.5 standard deviation of threshold voltage), SnP_2S_6 could become a potential candidate to construct advanced optoelectronic and electronic devices.

Methods

Material Characterization. Raman spectra is obtained in a Horiba confocal Raman system with an excitation laser of 532 nm. The morphology characterization and thickness calibration of the SnP_2S_6 film as well as thickness measurement of h-BN and MoS_2 are carried out with optical microscope and AFM instruments.

Fabrication of SnP_2S_6 phototransistor and SnP_2S_6/MoS_2 FET devices. The SnP_2S_6 phototransistor was fabricated by exfoliating the thin flakes onto heavily doped silicon substrates. The top electrodes are defined using standard photolithography process followed by thermal evaporation of the Ti/Au metal, and lift-off process. We have built three batches of SnP_2S_6/MoS_2 devices on Si/SiO2 substrate and on h-BN substrate, respectively. Thin-film 2D materials are obtained through a mechanical exfoliation process first. Then the 2D nanosheets of top-gate FETs are stacked up by polydimethylsiloxane (PDMS) assisted transfer technique onto h-BN nanosheet to develop heterostructures. And the source-drain and gate electrodes Ti/Au of every device were patterned and deposited by photolithography and a lift-off process. Preparation methods for other devices including back-gate FETs and top-gate FETs on different substrates vary according to their schematic.

Electrical and optical characterization measurements. We tested the device directly after fabrication. Electrical and optical characterization of devices consisted of I_D-V_G, I_D-V_D and I_{ph}-t characteristics. All measurements are performed under vacuum conditions at room temperature (300 K) using probe station.

Author contributions

J. H. and A. Z. carried out the electrical and optoelectronic measurement. E. P., J. C. and R. B. assistant the device fabrication and electrical measurement. E. P. carried out the AFM measurement. J. L. and X. J. carried out the Raman characterization. A. M. and Y. V. conducted dielectric measurement and crystal growth. Q. L., G. C. and P. M. analyzed the data. J. H., A. Z. and F. L. wrote the manuscript. Q. L. and G. C. and revised the manuscript. F. L. supervised the project. All the authors comments on the manuscript.

Conflicts of interest

There are no conflicts to declare.

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