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AD HOC DESIGN-FOR-TESTABILITY RULES

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When small-scale integration (SSI), medium-scale integration (MSI), and large-scale integration (LSI) were the dominant levels of component integration, large systems were often partitioned so that data flow paths and control circuits were placed on separate printed circuit boards (PCBs) [1]. Most PCBs in a given design contained data flow circuits that were not difficult to test using an ATPG. A lesser number contained the more complex control logic and handshaking protocols. Test programs for control logic would be created by requiring a logic designer or test engineer to write vectors that were then fault simulated to determine their effectiveness. Since the complex PCBs made up a smaller percentage of the total, test creation was not excessively labor-intensive. The task of writing tests for these boards [1] was further simplified by the fact that sequential transitions in control logic could often be observed directly at I/O pins rather than indirectly through observation of their effects on data flow logic.

The evolution of technology has brought about an era where individual ICs now possess hundreds of thousands to millions of gates. RAM and ROM often reside on the same IC with complex logic. Individual I/O pins serve multiple purposes, acting both as inputs and as outputs. The increasing gate to pin ratio results in fewer I/O pins with which to gain access to the logic to be tested. Architecturally, many chips have complex arbitration sequences that require several exchanges of signals before anything meaningful happens inside the chip. All of these factors contribute to potentially long test programs that strain the resources of available test equipment and point to the conclusion that test issues must be considered early in the design cycle.

It was pointed out in [2] that acceptable quality level (AQL) is a function of both the process yield and the thoroughness of the test program. If the process yield is high enough for a given product, it may not need a test, only an occasional sampling to ensure that processing steps remain within tolerances. Consider an IC for a digital wristwatch. It could be very expensive to test every chip for all stuck-at faults. But the yield on such chips is high enough that an occasional sampling of ICs is adequate to ensure that they will function correctly; and if an occasional defective IC slips through the screening process unnoticed, it is not likely to have severe economic consequences.

Ad hoc DFT addresses circuit configurations that make it difficult or impossible to create effective test programs, or cause excessively long test sequences. The adverse effects of these circuit configurations may be local, affecting only a few logic elements, or they may be global, wherein a single circuit construct causes an IC or PCB to become completely untestable. Some problems may manifest themselves only under adverse environmental conditions—for example, temperature extremes, humidity, physical vibrations, and so on. A solution to a particular problem is

sometimes quite simple and straightforward, the most difficult part of the problem being the recognition that there is a problem [1].

Testability problems for digital circuits can be classified as controllability or observability problems (or both). Controllability is a measure of the ease or difficulty with which a net can be driven to a known logic state. Observability is a measure of the ease or difficulty with which a logic value on a net can be driven to an output where it can be measured. Note that observability is often a function of controllability, meaning that it may be impossible to observe a given internal node if the circuit cannot be driven to (i.e., controlled to) a given state. Expressed in terms of controllability and observability, the goal of DFT is to make the behavior of a circuit easier to control and observe. We begin by looking at some circuit configurations that cause problems in digital circuits. That will be followed by an examination of techniques [2] used to improve controllability and observability. The solutions are often rather straightforward, and frequently there is more than one solution, in which case the solution chosen will depend on the resources available, such as the amount of board or die space and/or number of edge pins. Ad hoc solutions target specific test problems uncovered during the design and test process, and in fact similar test problems may be solved quite differently on different projects [1].

Literature

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